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**Amendments to the claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of claims:**

Claim 1 (currently amended): A method for fabricating a thermally-enhanced wafer-level chip scale package, comprising the steps of:

- (1) preparing a semiconductor wafer having a front side and a back side, and which is predefined into a plurality of integrated circuit chips, then proceeding to step (2);
- (2) ~~then~~ performing a bumping process to bond a plurality of solder bumps on the front side of the semiconductor wafer, then proceeding to step (3);
- (3) ~~then~~ performing a back-side lapping process to grind away a back-side portion of the semiconductor wafer, then proceeding to step (4);
- (4) ~~then~~ attaching a thermally-conductive stiffener to the back side of the semiconductor wafer by means of a thermally-conductive adhesive layer, wherein the thermally-conductive stiffener is free of electrical connection with the semiconductor wafer, then proceeding to step (5);
- (5) ~~then~~ performing a singulation process to cut the thermally-conductive stiffener and cut apart each chip from the semiconductor wafer, then proceeding to step (6); and
- (6) ~~then~~ performing a flip-chip die bonding process to mount each singulated chip by means of the solder bumps onto a circuited substrate.

Claim 2 (previously presented): The method of claim 1, wherein in said step (4), the thermally-conductive adhesive layer comprises silver epoxy.

Claim 3 (original): The method of claim 1, wherein in said step (4), the thermally-conductive stiffener is made of copper.

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Claim 4 (original): The method of claim 1, wherein in said step (4), the thermally-conductive stiffener is made of a copper alloy.

Claims 5-8 (canceled)